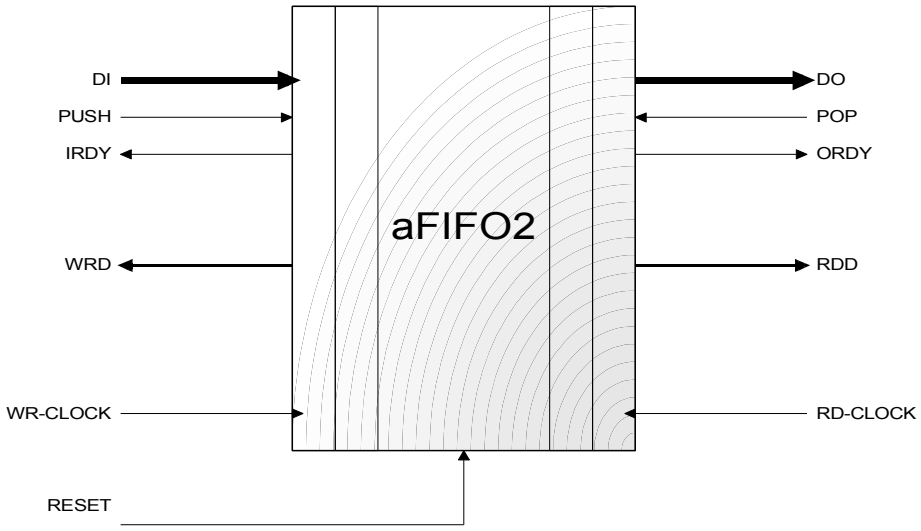
A2aFIFO

Asynchronous FIFO Alternate



aFIFO2 Symbol

FEATURES

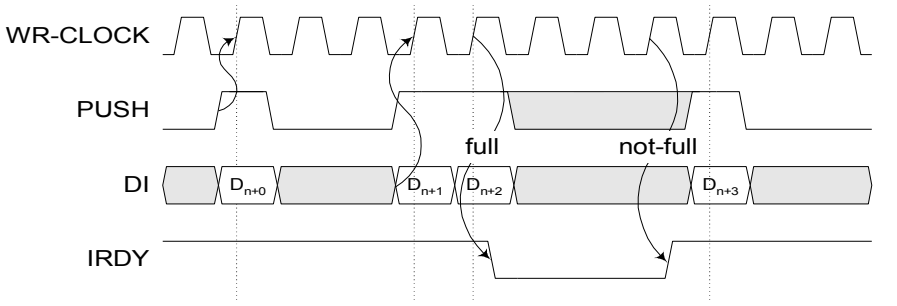
- Fully Synthesizable RTL - Verilog
- Static Timing Analysis compatible
- Dual-port inferred RAM architecture
- Configurable width and depth
- Standard FIFO handshake interface
- Insensitive to relative clockrates
- Flags or depth values on each port

APPLICATIONS

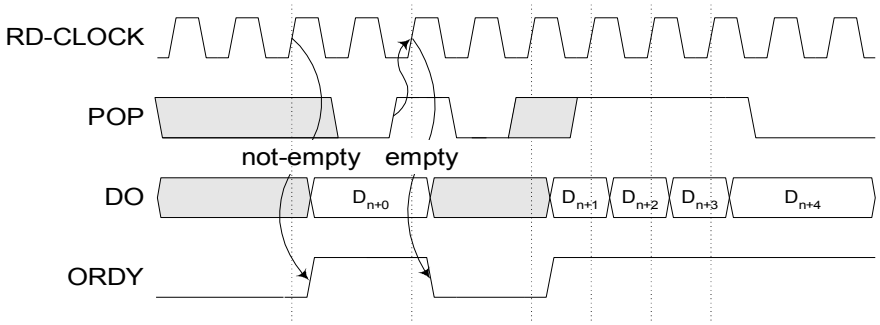
- Re-synchronizing data between clock domains
- General purpose buffering

The aFIFO2 controls are designed to ensure hazard free clock domain crossing between the read and write ports. Only single control lines are re-synchronized between the two clock domains ensuring hazard free operation. The requirement for Gray coded addressing is thus eliminated. A wide range of clock frequencies and relative frequencies between read and write ports are fully tolerated. The interface signals are fully synchronous to their respective domains; no asynchronous signals are present on either side. Only reset may be asynchronous in that it is asserted asynchronously and synchronized internally to both clock domains to again ensure hazard free operation.

Signal Name	Width	I/O	Description
Write Interface			
DI	Parameter	In	Data In
PUSH	1	In	Push Data Input the FIFO on next WR-CLOCK edge (rising or falling set by parameter)
IRDY	1	Out	Input Ready. FIFO is NOT full and can accept incoming data
WRD	Parameter	Out	Write Depth. Either a depth value or a parameter set depth threshold flag
WR-CLOCK	1	In	Write Clock
Read Interface			
DO	Parameter	Out	Data Out
POP	1	In	Pop Data Output from the FIFO on next RD-CLOCK edge (rising or falling set by parameter)
ORDY	1	Out	Input Ready. FIFO is NOT empty and is presenting data to be read
RDD	Parameter	Out	Read Depth. Either a depth value or a parameter set depth threshold flag
RD-CLOCK	1	In	Read Clock
System Interface			
RESET	1	In	Reset. Asynchronous Active, Synchronous Inactive



aFIFO2 Write Interface Timing



aFIFO2 Read Interface Timing