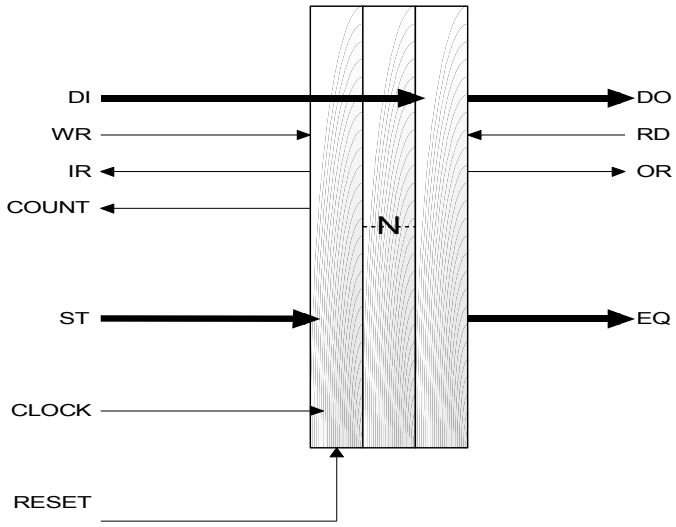
Advanced Architectures

A2 CAM-FIFO

Searchable FIFO



FIFO-CAM Symbol

FEATURES

- Fully Synthesizable RTL - Verilog
- Static Timing Analysis compatible
- Multiple Register for synchronous pipeline
- Configurable width
- Configurable overrun depth
- Standard FIFO handshake interface

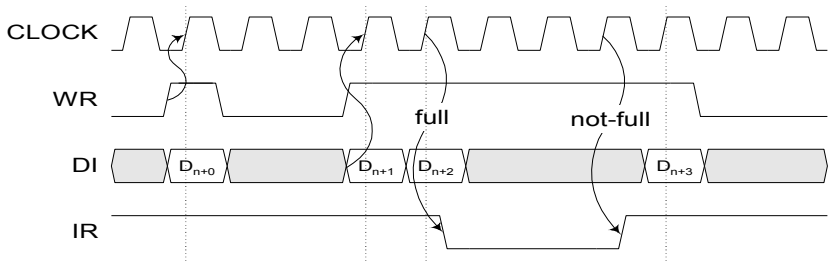
APPLICATIONS

- MMU Translation Buffer
- Tag buffer for tag based interfaces
- Credit buffer for credit based interfaces
- Small CAM
- Victim Cache
- Write Combining Buffer

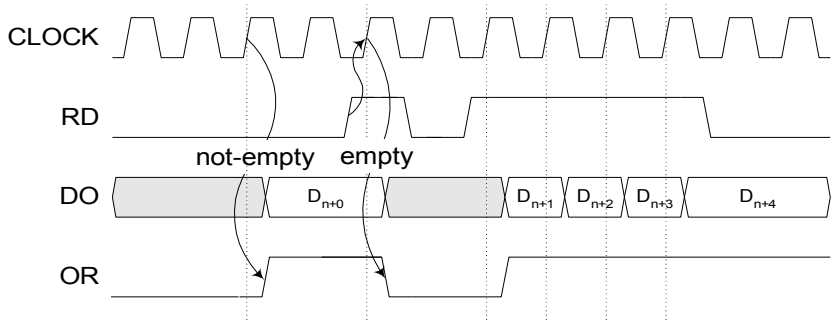
The FIFO-CAM controls are designed to operate over a wide range of clock frequencies. The interface signals are fully synchronous; no asynchronous signals are present on either side. Only reset may be asynchronous in that it may be asserted asynchronously and synchronized internally to the clock.

The contents of the FIFO buffer may be searched by a applying a search term to the ST input. If a match is found a bit-map of those locations that match are output on the EQ lines. This interface is asynchronous there being no registers within this datapath.

Signal Name	Width	I/O	Description
Write Interface			
FCM_DI	Parameter	In	Data In
FCM_WR	1	In	Push Data Input the FIFO on next WR-CLOCK edge (rising or falling set by parameter)
FCM_IR	1	Out	Input Ready. FIFO is NOT full and can accept incoming data
FCM_COUNT	Parameter	Out	A count of the number of FIFO locations occupied by valid data
Read Interface			
FCM_DO	Parameter	Out	Data Out
FCM_RD	1	In	Pop Data Output from the FIFO on next RD-CLOCK edge (rising or falling set by parameter)
FCM_OR	1	Out	Output Ready. FIFO is NOT empty and is presenting data to be read
Search Interface			
FCM_ST	Parameter	In	Search Term - same width as the data ports
FCM_EQ	Parameter	Out	Equal bits - One bit per register (pure combinatorial path from ST to EQ)
System Interface			
RESET	1	In	Reset. Asynchronous Active, Synchronous Inactive
CLOCK	1	In	System Clock



FIFO Write Interface Timing



FIFO Read Interface Timing