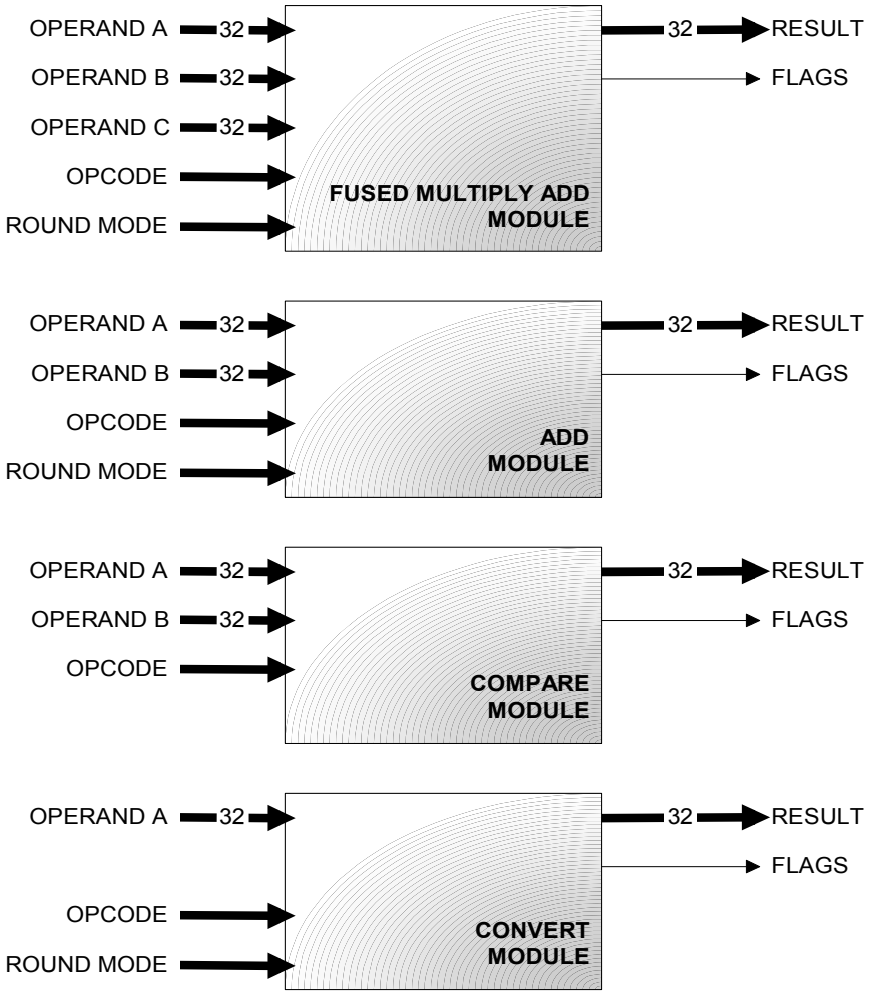

FEATURES

- IEEE-754 compliant (except underflow)
- Flush to zero underflow implementation
- Single precision
- Fused Multiply Add Module (5 STAGE PIPE)
  - Floating Point Multiply
  - Floating Point Amultiply-Add
  - 32-bit integer signed/unsigned
  - 32-bit integer signed round & shift
  - 32-bit integer signed and shift
  - 32-bit integer signed absolute result
- Add Module (5 STAGE PIPE)
  - Floating Point Add / Subtract
- All IEEE rounding modes supported
- **All IEEE exception flags supported**
- Compare Unit (1 STAGE PIPE)
  - Floating Point Compare
  - Floating Point min/max/saturate
  - Floating-point NAN test
  - Floating-point Absolute Value
- Conversion Module (2 STAGE PIPE)
  - Convert floating-point to/from integer

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OVERVIEW

The A2FM product is a collection of floating-point execution units compliant with the *ANSI/IEEE Std 754-1985, IEEE Standard for Binary Floating-Point Arithmetic* (IEEE-754 Standard). The units are designed for high frequency, high throughput implementations. Each unit is implemented as a state-less pipeline that can easily be integrated into a high-performance processor design.

Each unit is targeted for a clock cycle with only 10-12 gate delays (excluding setup and clock skew). The add and multiply units implement 5-cycle pipelines. The conversion unit implements a 2-cycle pipeline, and the compare unit a 1-cycle pipeline. All units can sustain a 1-cycle throughput.

The multiply unit supports fused floating-point multiply add, as well as a variety of 32-bit integer multiply functions.

IEEE-754 Compliance

The A2FM modules are designed to provide a powerful floating-point capability while minimizing die size cost. To minimize unnecessary design size, some of the rarely used features of the IEEE specification are not implemented directly in the hardware design. The following IEEE-defined operations are not directly supported in A2FM hardware, but can be supported with software support:

- Gradual Underflow
- Denormal Numbers

In place of gradual underflow, the A2FM modules implement a flush-to-zero approach when underflow occurs. This feature allows the A2FM modules to maintain a one-cycle throughput in all operand cases, and minimizes design size.

Performance

All modules are pipelined and can start a new function every cycle

Fused Multiply-Add unit:	42,000 NAND Gates	Throughput	1	Latency	5
Add unit:	12,000 NAND Gates	Throughput	1	Latency	5
Convert Unit:	6,600 NAND Gates	Throughput	1	Latency	2
Compare Unit:	1,400 NAND Gates	Throughput	1	Latency	1

Timing: 1 GHz clock on 45nm technology has been achieved

NOTE: The above performance data are estimates only, based on sample implementations using worst-case conditions. Achieved performance is highly dependent on the process technology, cell library, and synthesis tools used.

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