



Advanced Architectures

A2X : Interface Adapter Core for PCI-X

Overview

The A2X is a fully synthesizable module implemented in Verilog RTL. A2X functions as a complete PCI-X or PCI interface adapter in an ASIC. All aspects of PCI-X 2.0 (mode 1) and PCI 2.3 protocols and timing are handled by the A2X, leaving ASIC designers to interface to the core via a simple ASIC core-clock synchronous interface.

The A2X not only implements the state machine and data path required for PCI-X or PCI bus level handshaking; it also incorporates logic and queue/buffer structures for managing complex operations like Split Transaction, Delayed Read, Target read data prefetch etc.

A2X implements the PCI Configuration Space and enables address decoding through these registers. PCI or PCI-X bus is permitted to run only at particular frequencies, e.g. 33 Mhz, 66 Mhz, 100 Mhz or 133 MHz. An ASIC core-logic may however be desired to be operated by an independent clock, in most cases at much higher frequency, which is completely asynchronous to that of PCI or PCI-X bus clock. A2X makes that possible by incorporating two completely asynchronous clock domains inside it. Transactions are packetized and forwarded across the clock domains via command queues and data buffers internal to A2X. Thus the ASIC core interface and the PCI/PCI-X interface could be clocked by completely independent clock sources.

Standard interfaces can be supplied on the ASIC side including, but not limited to, A2B, OCP, BVCI, AVCI and AMBA.

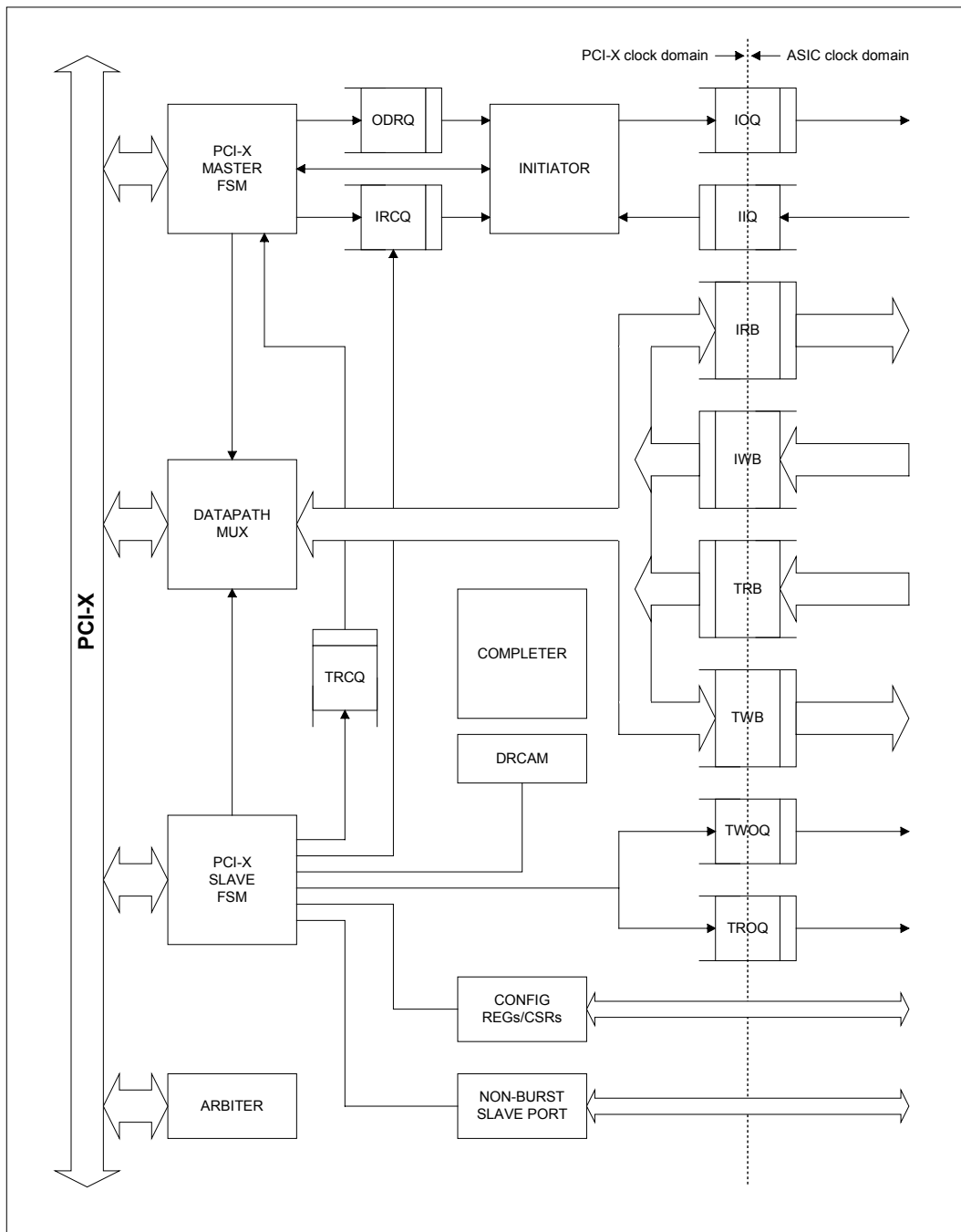
A full suite of diagnostic and verification testbenches is supplied with the core together with a PCI compliance checklist.

Feature List

- PCI-X 2.0 mode 1 compliance
- PCI 2.3 compliance
- Complete protocol isolation and high performance datapath pipelining
- Dual independent clock domains with interface queues
- Supports 66MHz to 133MHz PCI-X and 33MHz to 66MHz PCI timing
- 64/32-bit PCI-X interface
- 64/32-bit PCI interface
- Supports up to 32 outstanding Initiator mode Split transactions (Sizeable)
- Supports up to 32 outstanding Target mode Split transactions (Sizeable)
- Supports up to 32 outstanding Target mode Delayed Read (Sizeable)
- Supports up to 4 outstanding Initiator mode Delayed Read (optional)
- Read and Write buffers and command/response queues for Initiator & Target (Sizeable)
- All storage structures implementable as either SRAM or Reg file or bit-by-bit FFs
- Incorporates asynchronous interface between PCI-X clock domain and ASIC core clock domain via above buffers and queues
- Simple synchronous interfaces to ASIC core:
- Separate full duplex burst ports for Initiator and Target packets.
- 128/64-bit data width for burst ports
- A separate non-burst Configuration Registers / internal CSR access port with 32-bit data width
- A non-burst target port with 32-bit data width
- Stand alone PCI/PCI-X single stage, 4 way round robin arbiter
- Type 0 base Configuration Header Registers included
- PCI-X Capabilities list item registers included
- Target address decode via Configuration regs
- Interrupt delivery mechanism
- Interrupt ACK and Special cycles supported
- Dual Address Cycle or DAC supported
- MSI not supported
- EPROM support via target non-burst port
- Special handling of Target Memory Write with byte enables

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