



### Overview

A2R provides an interconnection mechanism between control registers in an ASIC design and any number of control devices; CPUs, debug ports etc.. The bus is especially suited for synthesizable designs. It is specifically developed to meet the challenges of long interconnect delays in large System-on-chip designs and can be tailored to match system clock rates.

A2R is a fully synchronous auxiliary bus that is user configurable to provide a wide variety of performances to best match the system level requirements of a particular implementation. The user (system architect) can configure the system for address and data widths, may add special bus fields to transfer custom information and may select the arbitration algorithm. Bridges (called Gateways) can also be included to allow different bus sections to operate independently. In order to access through the gate an initiator signals the gateway to request the upper level bus and send its access upwards. This mechanism allows the initiators in separate segments to access within their segment at any time and only at a higher level through a higher-level arbitration.

Local interconnections between sub-modules are often configured using an OR structure as the A2R fabric and inter-module connections are configured to use a ring structure. This point-to-point topology can then be pipelined so that all sections of the ring settle within a single clock cycle this allows the A2R to be configured such that only single cycle operations exist and no false path or multi-cycle paths exist which significantly eases timing closure in large SoC designs.

### Feature List

#### Data Paths

- Multiplexed address and data bus for minimum interconnect
- 8, 16, 32 ... or any width of address and data bus
- Custom bus widths may be specified

#### Protocols

- Simple master and target interfaces
- Clock rate independent protocols
- Single protocol for all performance levels
- Multiple master and target capability
- Multi-segment capability
- Direct attach of ARC host and auxiliary buses

#### Addressing

- Customizable assignment of address space
- ARC debug compatible

#### Devices

- Any number of transaction initiators
- Any number of transaction targets

#### Arbitration

- User configurable/customizable
- Base algorithms provided
  - Round-robin

#### Fabric

- Parallel OR-gate multiplexing
- Serial point-to-point
- Pipelined point-to-point

#### Bridges (Gateways)

- On-chip between segments

#### Interfaces

- Initiator and Target TAPs
  - Simple synchronous protocol
  - Clock domain transition support
- Industry standard veneers
  - A2B, OCP-IP
  - VSIA (BVCI, PVCI), AMBA on request

#### Extensions

- Parity protection
- Error protocol
- User-defined bus fields
- Bus monitoring

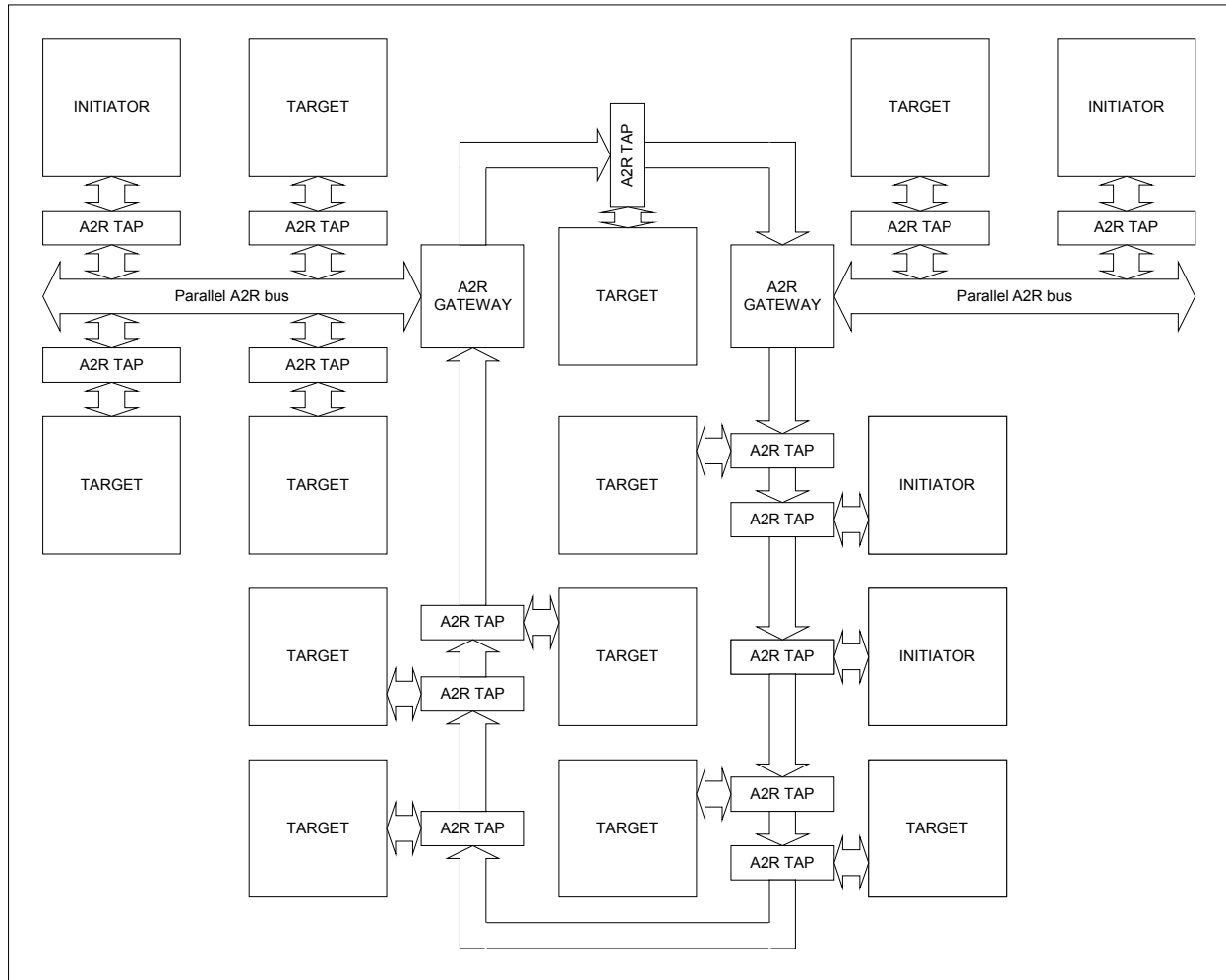


Figure 1 Sample A2R configuration for a System-on-Chip

**Disclaimer:** Information furnished by Advanced Architectures is believed accurate and reliable. Advanced Architectures reserves the right to change specifications detailed in this datasheet at any time, without notice, in order to improve reliability, function or design and assumes no responsibility for any errors within this document. Advanced Architectures does not make any commitment to update this information. Advanced Architectures assumes no obligation to correct errors contained herein or to advise any user of this text of any correction, if such be made, nor does Advanced Architectures assume responsibility for the function of un-described features or parameters.

No license is granted by implication or otherwise under any patent or patent rights of Advanced Architectures.

Copyright © 2003, Advanced Architectures.

Advanced Architectures contact info:

[www.a-2.com](http://www.a-2.com)

Advanced Architectures  
 19421 Sierra Lago Road  
 Irvine CA 92612-3812  
 +1 949 412 3486