Advanced Architectures

A2P

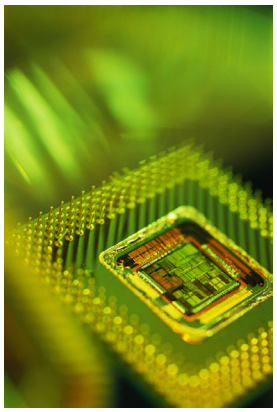
Configurable High performance Processor Family

32/64-bit Application Adaptive Processor

Features

- High performance
- 16-bit expandable Instruction Set
- 32-bit and 64-bit versions
- 400 MHz in 0.13µm process
- Extreme low-power using demand clocking scheme
- Extreme small size. Base A2P about the size of an 8051

The A2P processor family provides a range of processors all based on a common instruction set. This instruction set is readily expandable to cover a wide variety of applications. Additional functionality may be crafted for a precise match with the final product. DSP, floating point, SIMD and custom extensions simply plug-in to the core. Equally unused functionality may be removed. Various processor core models focus on area, power and performance to ensure an optimal fit.



The A2P is agnostic to interconnect types and maybe attached to any standard including Advanced Architectures' A2B system interconnect that supports multiprocessor configurations with various coherent memory architectures as well as network on chip topologies.

Applications

Network
Protocol Offload
Packet Processing
Security

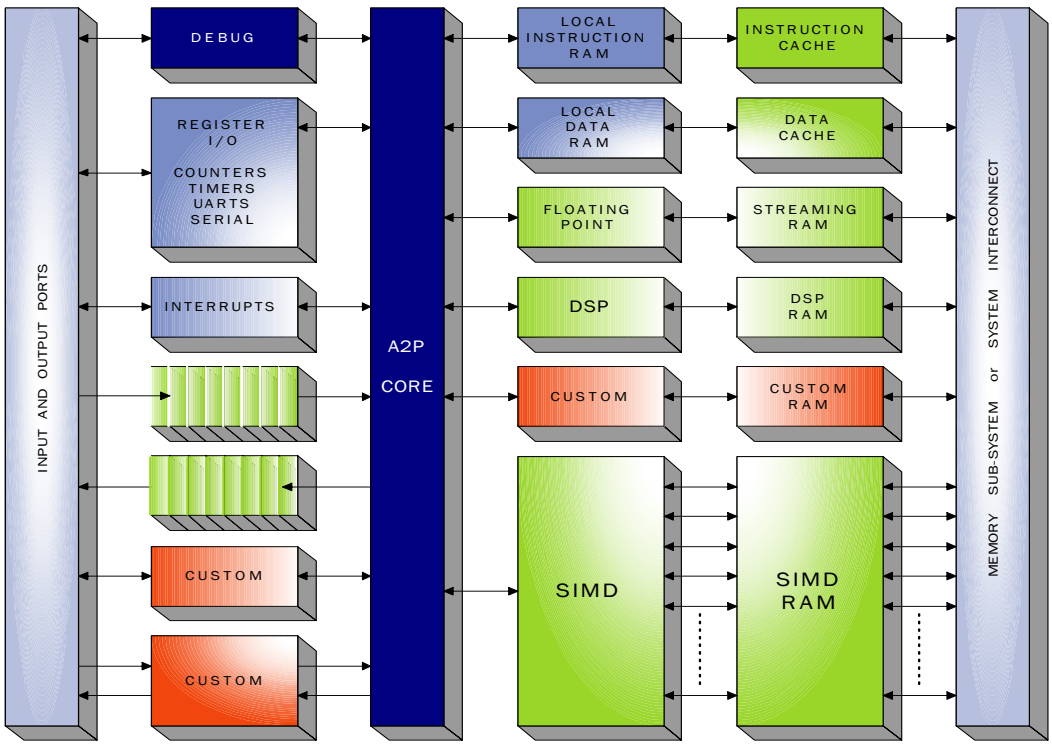
Portable
Audio / Video player
GPS, Cellular
Camera

Storage
Disk Drives
SAN / NAS
RAID

Signal & Image
Imaging
Recognition
Tracking

Consumer
Set-top boxes
Gaming
HDTV
DVR, DVP

A2P



A2P Architecture

Processor Architecture

- Multi-cycle, Single-cycle and Superscalar core variants
- 16-bit expandable instruction set
- 32-bit or 64-bit address and data
- 32, 64 or 128-bit data buses
- Hierarchical Register Sets
- Multiprocessing support
- Configurable interrupt unit
- User and Supervisor modes with privilege levels

Standard Plug-ins

- Instruction and data caches
- Single/Double Precision Floating point
- Streaming RAM for vector FPU
- DSP ALU with MAC including saturating arithmetic
- DSP RAM supporting multi-port or XY memories
- Configurable SIMD engine supporting 64 to 2048-bit width. Floating Point capable
- High speed FIFO based direct I/O
- Memory Management with TLBs

Tools

- Unified HW/SW co-verification
- Cycle accurate ISA simulator
- Verilog and System C simulation support
- Multi-target debug ISS, RTL & HW
- Multi-core complete IDE with C compiler
- Windows & Linux

The A2P provides a base set of instructions that form the core requirements for a processor and a configuration mechanism that allows the simple incorporation into the instruction set of specialized instructions that optimally execute a given range of applications. The determination of the specialized instructions is derived from careful profiling of applications intended for a given embedded solution space.

A Profiling tool is a system level design environment which enables designers to quickly analyze their architecture and modify their system for optimal performance.

Most systems consist of processors, caches, memories, interconnect, peripherals, function blocks, and software algorithms. It is critical for the architecture to support the efficient flow of data between the blocks to meet the performance requirements of the system. The profiling tool provides the capabilities critical to the designer for developing a robust and efficient solution. The tool utilizes a high speed Instruction Set Simulation environment. The hardware/software co-simulation enables the tool to collect key system performance measurements.

These measurements identify the bottlenecks in the architecture which are limiting performance. The tool also performs software profiling. These measurements pinpoint inefficiencies in the design and enable the concurrent optimization of the system architecture, the hardware and the software. The tool models the complete memory hierarchy which may include cache memories, write buffers, RAMS, flash memories, etc. Using these data the memory subsystem can be configured to achieve optimal performance

The thorough understanding gained of the hot spots of the profiled algorithms is used to optimize the existing code and then to develop custom instructions as necessary to meet the goals of a particular solution. This may be a performance goal, a power goal, a silicon area goal, or most likely a combination of all three. These instructions are then integrated into the A2P processor design and the software toolset, and most importantly, the C compiler, are retargeted to the modified processor. The resulting system is then re-profiled to determine the resultant benefit to ensure that the design goals are met.

This process allows for the customization of hardware and software to a given application space and provides an optimal solution for a given specification. The primary benefits are reduced cost, improved performance, increased security and protection of IP. As the system is customized to a unique processor with a unique instruction set the possibility of reverse engineering the product is made significantly harder. Further as the system is a custom design any software brought into the system, can be highly encoded so long as a decoding mechanism is also built-in.

The result is optimized software that uses the minimum amount of code space and CPU cycles to perform a given algorithm or range of algorithms and a hardware design that executes these software programs in a most efficient manner for a set of power, area and performance criteria.

Phone: 949 412 3486
Fax: 949 856 3034
E-mail: sales@a-2.com
Website: www.a-2.com