A2B: Synchronous System Bus

Advanced Architectures

Overview

A2B is a high performance system bus designed for use in synthesizable designs. It is specifically developed to meet the challenges of multiprocessor and multiple DMA / IO processor, System-on-chip designs. A2B is designed to have the highest possible bus occupancy so that the sustainable bus bandwidth closely approaches the available peak bandwidth of a given configuration.

A2B is a fully synchronous system bus that is user configurable to provide a wide variety of performances to best match the system level requirements of a particular implementation. The user (system architect) can configure the system for address and data widths, may add special bus fields to transfer custom information and may select the arbitration algorithm. Bridges can also be included to allow different bus widths in separate sections so that a variety of devices can connect together. This allows, for example, a collection of CPUs to have a very wide bus connection to system memory and for slower I/O devices to have a narrower bus connecting through the bridge to the system memory.

Feature List

Data Paths
- (Any power of 2)-bit Read & Write data bus
- Any size Address bus
- Custom, user-defined buses

Protocols
- True split transaction reads
- Split read and write buses
- Clock rate independent protocols
- Multiple byte and burst modes
- Tagged transactions for secure operation
- Single protocol for all performance levels

Addressing
- Customizable assignment of address space
- Big-endian and little-endian support

Devices
- Any number of transaction initiators
- Any number of transaction targets

Arbitration
- User configurable/customizable
- Base algorithms provided
  - Simple priority
  - Round-robin
  - Multiple levels
- Rate limiting per initiator per segment

Fabric
- Parallel OR gate multiplexing
- Serial OR gate pseudo-three-state
- Point-to-Point
- Crossbar switching for highest performance

Bridges
- On-chip between segments
  - supports different bus widths
- Off-chip

Interfaces
- Initiator and Target TAPs
  - optional FIFO buffering
  - simple synchronous protocol
  - separate clocking support
- Industry standard veneers
  - OCP-IP
  - VSIA (AVCI, BVCI)
  - AMBA

Extensions
- Parity protection on any and all buses
- Virtual addressing and translation
- Central address translation support
- Address burst and complex addressing
- Multiprocessor protocols
  - Interlock
  - Cache coherency via SNOOP
  - Cache coherency via Directory
- Error and Retry protocols
- User-defined bus fields
- Bus monitoring

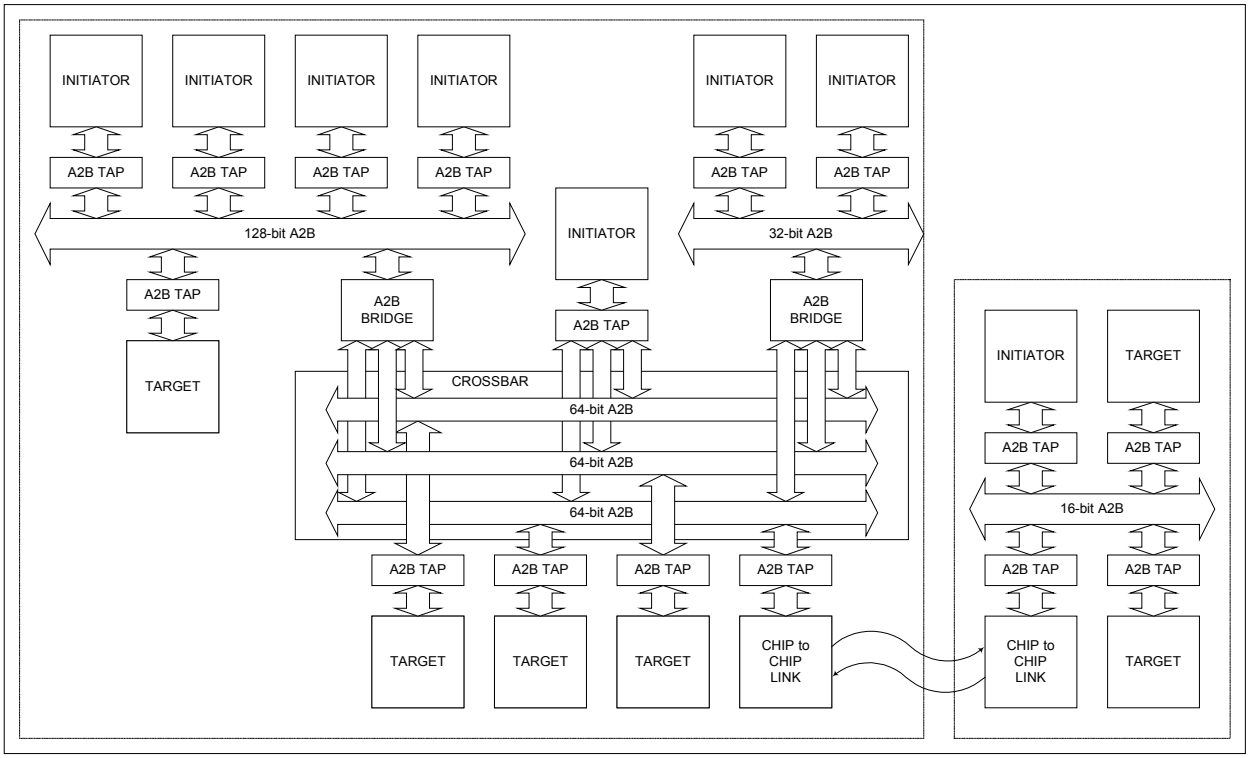

Figure 1 Complex A2B structure across 2 chips

Performance

The table below gives the performance for a target clock speed of 200 MHz, which is readily achievable at 0.18µm technology for a single segment of A2B. Note that actual figures are entirely dependant on the characteristics of a particular technology, operating parameters and synthesis constraints.

	32-bit datapath	128-bit datapath	1024-bit datapath
peak bandwidth per data bus	800 Mbytes/second	3.2 Gbytes/second	25.6 Gbytes/second
peak system bandwidth	1.6 Gbytes/second	6.4 Gbytes/second	51.2 Gbytes/second

Configuration

The A2B is configurable to generate a wide variety of topologies to best suit an individual application. The configuration is table-driven and an appropriate hierarchy is built so that the interconnection fabric exists on the upper layers of the system hierarchy and the TAP modules reside in the modules that they interface to. The resulting bus structure will also have a companion testbench and verification suite that allows the incremental addition of user modules to build a complete system.

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